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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/444,675	11/22/1999	TORU KOIZUMI	35.C14029	8958

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EXAMINER	
WU, DOROTHY	

ART UNIT	PAPER NUMBER
2615	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/444,675	KOIZUMI ET AL.	
	Examiner	Art Unit	
	Dorothy Wu	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) 10-20 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-9 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The substituted specification has been received and entered.

Response to Arguments

2. Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection.

Response to Amendment

3. Acknowledgement is made of the amendment to claim 6. The 35 USC 112, 2nd paragraph rejection of claim 6 is hereby withdrawn.

4. Because the applicant did not traverse the office's use of Official Notice in the previous Office Action, the teaching that it is well known to separate pixel data into luminance and chrominance components is therefore accepted as prior art.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shintani, U.S. Patent 5,875,034, in view of the admitted prior art.

Regarding claim 1, Shintani teaches a sensor comprising a sensor block (CCD) including a pixel unit comprising a plurality of pixels each including a light-receiving element and a signal processing block (signal processing unit 102) for processing a signal output from said sensor block (col. 7, lines 26-31). As the CCD outputs pixel information to the signal processing block, a scanning unit for selecting a pixel of said pixel unit is inherently taught. Shintani teaches a single electric power voltage input terminal for externally inputting an external power voltage (main battery EB in power supply unit 109) from outside of the sensor (Fig. 2A, col. 7, 56-58); and a control circuit (DC/DC converter 200) for generating a plurality of different voltages from the electric power voltage (main battery EB in power supply unit 109) externally input at the single electric power voltage input terminal (col. 9, lines 7-25). Shintani teaches that the power supply unit 109 is adapted for supplying a high voltage of a predetermined level to the CCD 101, and a lower voltage of a predetermined level to other individual circuit elements (col. 7, lines 52-55), which reads on a power supply voltage used in a sensor block that is higher than a power supply voltage supplied to another individual circuit element. It would have been obvious to one of ordinary skill that the other individual circuit elements would include the signal processing unit. Shintani does not teach that the sensor is integrated on a single semiconductor substrate. The admitted prior art teaches a sensor integrated on a single semiconductor substrate (page 1, lines 10-12). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the practice of fabricating camera elements on a single integrated chip taught by the admitted prior art into the camera of Shintani. One of ordinary skill

would have been motivated to make such a modification to shorten the time needed to transport pixel data from the image sensor to the signal processing unit.

Regarding claim 5, the admitted prior art teaches that the light-receiving element is a buried photodiode (page 2, line 5). One of ordinary skill would have been motivated to use the buried photodiode of the admitted prior art in the sensor of Shintani to obtain a signal with a higher S/N ratio.

Regarding claim 8, Shintani teaches an A/D converter for converting the signal (Fig. 4A, item 305). It would have been obvious to one of ordinary skill to incorporate the A/D conversion into the signal processing block.

6. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shintani, U.S. Patent 5,875,034, in view of the admitted prior art, and further in view of Mann et al, U.S. Patent 6,121,087.

Regarding claim 2, Shintani in view of the admitted prior art teach the apparatus of claim 1. See above. Shintani in view of the admitted prior art do not teach that a gate insulating layer of at least some insulated gate transistors of said sensor block is thicker than that of an insulated gate transistor used in said signal processing block. Mann et al teaches that the application of a higher voltage will require a thicker gate oxide layer to prevent oxide breakdown (col. 6, lines 34-42). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the practice of growing a thicker oxide when a higher voltage is being applied taught by Mann into the apparatus of Shintani in view of the admitted prior art to make an image sensing apparatus that uses a higher power voltage, and thus thicker gate oxide

layers, for the sensor block and a lower power voltage, and thus thinner gate oxide layers, for the signal processing block. One of ordinary skill would have been motivated to make such a modification to fabricate the appropriate thickness of oxide for the voltage that shall be used upon it.

7. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shintani, U.S. Patent 5,875,034, in view of the admitted prior art, in view of Mann et al, U.S. Patent 6,121,087, and further in view of Gardner et al, U.S. Pub. No. 2002/0022325.

Regarding claim 4, Shintani in view of the admitted prior art teach the apparatus of claim 1. See above. Shintani in view of the admitted prior art in view of Mann teach that the gate insulating layers of some transistors of said sensor block is thicker than that of an insulated gate transistor used in said signal processing block. See above. Shintani in view of the admitted prior art in view of Mann do not teach that a threshold voltage of at least some insulated gate transistors of said sensor block is higher than that of an insulated gate transistor used in said signal processing block. Gardner teaches that thinner gate oxides will require a lower threshold voltage [0008]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of having a lower threshold voltage when a transistor has a thinner gate oxide taught by Gardner into the apparatus of Shintani in view of the admitted prior art in view of Mann to make an image sensing apparatus whose transistors in the signal processing block use a lower power supply and possess a lower threshold voltage than the transistors on the signal processing block. One of ordinary skill would have been motivated to make such a modification to reduce the power consumption of the sensor block by

using different power supplies and reduce the fabrication time by growing thinner oxides that require lower threshold voltages.

8. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shintani, U.S. Patent 5,875,034, in view of the admitted prior art, in view of Mann et al, U.S. Patent 6,121,087, and further in view of Sawada et al, U.S. Patent 6,184,516.

Regarding claim 3, Shintani in view of the admitted prior art teach the apparatus of claim 1. See above. Shintani in view of the admitted prior art in view of Mann teach that the threshold voltages for the sensor block transistors are higher than the threshold voltages for the signal processing block transistors. See above. Shintani in view of the admitted prior art in view of Mann do not teach that the well density of at least some insulated gate transistors of said sensor block is lower than that of an insulated gate transistor used in said signal processing block. Sawada teaches a pMOS transistor 323 is formed on an n type well 19 whose impurity concentration is higher than that of the n type semiconductor substrate on which the n type well 19 is formed, and a pMOS transistor 324 is formed outside of the n type well 19 on the n type semiconductor substrate. The threshold voltage of pMOS transistor 323 formed on the n type well 19 is about -0.75 V, and that the threshold voltage of the pMOS transistor 324 formed outside of the n type well on the n type semiconductor substrate is about -0.29V (col. 6, lines 61-col. 7, line 8). Therefore, Sawada teaches that the transistor formed in a substrate possessing a lower well impurity concentration will have a higher threshold voltage. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of fabricating a transistor in a substrate with a lower impurity concentration to achieve a

higher threshold voltage taught by Sawada with the apparatus of Shintani in view of the admitted prior art in view of Mann to make an image sensing apparatus whose signal processing block transistors use lower voltage, possess thinner gate oxide layers, and are fabricated in wells of lower impurity concentration than those of the transistors on the signal processing block. One of ordinary skill would have been motivated to make such a modification to reduce the overall power consumption of the chip.

9. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shintani, U.S. Patent 5,875,034, in view of the admitted prior art, and further in view of Tandon et al, EPO 0 254 497.

Regarding claim 6, Shintani in view of the admitted prior art teach the apparatus of claim 5. See above. Shintani in view of the admitted prior art do not teach that each pixel has a charge/voltage conversion unit connected to the buried photodiode through a transfer switch. Tandon does teach that each pixel has a charge/voltage conversion unit (source follower 33) connected to a photodiode (14) through a transfer switch (phi.1) (col. 3, lines 25-32). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the charge/voltage conversion unit and transfer switches of Tandon into the apparatus of Shintani in view of the admitted prior art to make an image sensing apparatus that uses a lower power supply for the signal processing block than the sensor and converts the photoelectric charge accumulated in the pixels into voltage when the charge is transferred. One of ordinary skill would have been motivated to make such a modification to control when the charges are transferred and converted to voltages.

10. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shintani, U.S. Patent 5,875,034, in view of the admitted prior art, and further in view of Vu et al, U.S. Patent 6,025,875.

Regarding claim 7, Shintani in view of the admitted prior art teach the apparatus of claim 1. See above. Shintani in view of the admitted prior art do not teach that the sensor block and signal processing block are connected via a level shift circuit for shifting a signal level. Vu teaches that the sensor block and signal processing block are connected via level shift circuit (coupling capacitor C_{CL}) for shifting a signal level (col. 4, lines 9-13). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the level shift circuit of Vu into the apparatus of Shintani in view of the admitted prior art to make an image sensing apparatus that supplies different voltages to the CCD and signal processor and uses a level shift circuit or shifting a signal level between the CCD and signal processor. One of ordinary skill would have been motivated to make such a modification to reduce signals' voltage level when they are to enter another functional unit that employs a lower voltage supply.

11. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shintani, U.S. Patent 5,875,034, in view of the admitted prior art, and further in view of well-known prior art.

Regarding claim 9, Shintani in view of the admitted prior art teach the apparatus of claim 8. See above. Although Shintani in view of the admitted prior art do not teach a circuit for forming a luminance signal and a chrominance signal, the office takes Official Notice that it would have been obvious to one of ordinary skill in the art at the time the invention was made to

separate the image data of Shintani in view of the admitted prior art into luminance and chrominance signals. One of ordinary skill would have been motivated to make such a modification to convert the image data into a format that is commonly used in signal processing methods.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dorothy Wu whose telephone number is 703-305-8412. The examiner can normally be reached on Monday-Friday, 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Christensen can be reached on 703-308-9644. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dorothy Wu

DW
May 13, 2004

ANDREW CHRISTENSEN
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